AMENDMENTS TO THE SPECIFICATION

Please insert the following paragraph after line 12 of page 3:

Fig. 4A shows additional details of the DAC shown in Fig. 4 consistent with at least one embodiment of the invention.

Please replace the paragraph beginning at page 8, line 15 with the following amended paragraph:

Turning now to additional details of one embodiment of the invention, a functional diagram of the high-speed register 115 is shown in Figure 3. The high speed register block includes an amplifier 301 with a programmable offset 303, and a differential-input/single-ended-output register 305. Figure 4 shows additional details of the programmable offset amplifier 301. The amplifier includes [[~~of~~]] a Gm-R stage with two degenerating resistors 402. A constant bias current 404 is connected to the virtual ground node between the two degenerating resistors 402 and the source nodes of the input NMOS transistors 405 and 407 are connected to the output of a digital-to-analog converter (DAC) 409. The DAC 409 converts the digital input word, LOS threshold 127, into a differential current, ($I_{RIGHT} - I_{LEFT}$). That differential current changes the offset of the amplifier.

Please replace the paragraph beginning at page 10, line 11 with the following amended paragraph:

In one embodiment, referring again to Fig. 4, because of the limited monotonicity that could be provided by a single digital to analog converter, DAC 409 actually is comprised of two DACs, a coarse DAC and a fine

DAC (Fig. 4A). If a single DAC is used, in which the DAC is implemented using transistors in which the ratio of the sizes is binary, a transition from one digital code, e.g., 011111 to 100000 may result in a lower current rather than a higher current because of, e.g., process variations in the transistors. Thus, there is a risk that the DAC output would not be monotonic. In one solution to this problem using two DACs, each DAC is utilized during the calibration routine as follows. The fine grained DAC is set to its midpoint and the coarse grained DAC, which receives four bits, is operated for a period of time (e.g., 16 samples) without averaging but counting the up/down counter according to the output of the subsampler 123, which allows the DAC to come close to its proper state. Then an additional number of samples (e.g.,16) are taken and a setting for the coarse grained DAC is selected based on an average of those samples.

Please replace the paragraph beginning at page 13, line 15 with the following amended paragraph:

The count threshold can be adjusted ~~according~~ to account for noise and bandwidth limitations. The bandwidth limitations result in gain degradation at high frequency. Thus, if the LOS threshold is set relatively high, for example 30 mV peak to peak, the bandwidth limitation effects present in the high-speed register may result in being able to see only 24 mV. Assuming noise is on the order of 0.5 mV, the [[~~and~~]] gain degradation of 6 mV is the dominant effect and not the noise, so the noise does not have to be averaged out. Further, the signal degradation due to bandwidth limitations can result in a lower number of ones. Thus, based on the LOS level, the count threshold can be adjusted to, e.g., 2 rather than 15. On the other hand, at low LOS levels, the noise is at least as dominant as the bandwidth limitation effects and needs to be averaged out. Thus, the count threshold is increased to, e.g., 15. For LOS levels

that are in the middle, the count threshold would be adjusted accordingly. In one particular embodiment, the LOS threshold is divided into four ranges: 0-6 mV, 6-9 mV, 9-13 mV and 13-30 mV with corresponding count thresholds of 18, 14, 8, and 3, respectively.